Inconsistencies in the Examiner's Arguments

In rejecting claim 1, the Examiner relied upon Fig. 1 in Muza. The Applicant notes that there are certain inconsistencies in the Examiner's arguments that make it difficult to interpret the Examiner's reasons for rejecting claim 1. For example, in paragraph 3 on page 2, the Examiner indicated first that M3 is the first load device of claim 1, but two lines later, the Examiner indicated that M12 is the first load device. In paragraph 3 on page 2, the Examiner indicated that M11 is the first inductance-creating element of claim 1, but in the first line on page 3, the Examiner indicated that M12 is the first inductance-creating element. As best understood, the Applicant assumes that the Examiner believes that M3 is the first load device and that M12 is the first inductance-creating element.

The Examiner also indicated in the last line of page 2 that D1 is the power-supply rejection element of claim 1. Since D1 is a node, the Applicant assumes that the Examiner believes that transistor M_{B1} is the power-supply rejection element.

In the second-to-last line of page 2, the Examiner indicated that A1 is the first output node of claim 1, but in the second line of page 3, the Examiner indicated that A2 is the first output node. Since node A2 is in Fig. 2, not Fig. 1, the Applicant assumes that the Examiner intended to refer to A1 on page 3.

When rejecting claim 2 and again when rejecting claims 5 and 9, the Examiner referred on page 3 to Muza's Fig. 2. The Applicant assumes that the Examiner intended to refer to Muza's Fig. 1.

When rejecting claims 5 and 9, the Examiner also indicated on page 3 that the voltage at "the input gate of M11, M12" is the sensed common-mode voltage signal of claims 5 and 9. As best understood, the Applicant assumes that the Examiner believes that the voltages at the input gates of M11 and M14 form the sensed common-mode voltage signal.

The Applicant requests clarification if any of these assumptions are not correct.

Mischaracterizations in the Examiner's Arguments

Claim 1

Claim 1 is directed to circuitry comprising a first differential transistor pair connected between a first load device and a first current sink. A first inductance-creating element is connected to the first load device to add inductance at a first output node of the circuitry. A power-supply rejection element is connected between the first inductance-creating element and a first voltage reference to provide power-supply rejection at the first output node.

In the non-limiting, exemplary embodiments of Figs. 2-4:

- Transistors M6 and M7 form an example of the first differential transistor pair of claim 1;
- Transistor M4 is an example of the first load device of claim 1;
- Current source I_{total}-I_{neg} is an example of the first current sink of claim 1;
- Transistor M2 is an example of the first inductance-creating element of claim 1;
- VON is an example of the first output node of claim 1;
- Transistor M1 and current source I1 form an example of the power-supply rejection element of claim 1; and
- VDD is an example of the first voltage reference of claim 1.

In rejecting claim 1, the Examiner indicated, among other things, that (a) transistor M12 in Muza's Fig. 1 is an example of the first inductance-creating element of claim 1 and (b) transistor M_{B1} in Muza's Fig. 1 is an example of the power-supply rejection element of claim 1. For the following reasons, the Applicant submits that the Examiner mischaracterized the teachings in Muza in rejecting claim 1.

First of all, Muza's transistor M12 is not an inductance-creating element that adds inductance at Muza's node A1. Rather, Muza's transistor M12 is part of one of two differential pairs in Muza's common-mode error amplifier (consisting of transistors M5-M6 and M11-M14 and current sinks I2 and I3).

In order for Muza's transistor M12 to be an inductance-creating element that adds inductance at Muza's node A1, (1) node A1 would have to be connected to the source of transistor M12 and (2) a resistive device would have to be connected in series with the gate of transistor M12. Since Muza's circuitry does not satisfy these two conditions, transistor M12 cannot be an example of the inductance-creating element of claim 1. Further information on inductance-creating circuitry can be found in the discussions of the output impedance of source-follower circuits contained in textbooks on analog integrated circuit design.

Secondly, Muza's transistor M_{B1} is not a power-supply rejection element. In fact, transistor M_{B1} is a common-mode reference that actually follows the power supply. As such, transistor M_{B1} is essentially the opposite of a power-supply rejection element.

For at least these two reasons, the Applicant submits that the Examiner mischaracterized the teachings in Muza. As such, the Applicant submits that the rejection of claim 1 based on Muza is improper. Hamano does not teach the features in claim 1 that are missing from Muza.

The Applicant submits therefore that claim 1 is allowable over the cited references of Muza and Hamano. Since the rest of the claims depend variously from claim 1, it is further submitted that those claims are also allowable over the cited references. The Applicant submits therefore that the rejections of claims under Sections 102(e) and 103(a) have been overcome.

Claim 2

According to claim 2, a second load device is connected to the first differential transistor pair, and a second inductance-creating element is connected to the second load device to add inductance at a second output node of the circuitry, where the power-supply rejection element is connected between the second inductance-creating element and the first voltage reference to provide power-supply rejection at the second output node.

In the non-limiting, exemplary embodiments of Figs. 2-4:

- Transistor M5 is an example of the second load device of claim 2;
- Transistor M3 is an example of the second inductance-creating element of claim 2; and
- VOP is an example of the second output node of claim 2.

In rejecting claim 2, the Examiner also relied upon Fig. 1 in Muza. In particular, the Examiner stated, among other things, that transistor M13 in Muza's Fig. 1 is an example the second inductance-creating element of claim 2. For the following reasons, the Applicant submits that the Examiner mischaracterized the teachings in Muza in rejecting claim 2.

Similar to transistor M12, in order for Muza's transistor M13 to be an inductance-creating element that adds inductance at Muza's node B1, (1) node B1 would have to be connected to the source of transistor M13 and (2) a resistive device would have to be connected in series with the gate of transistor M13. Since Muza's circuitry does not satisfy these two conditions, transistor M13 cannot be an example of the inductance-creating element of claim 1.

For at least this reason, the Applicant submits that the Examiner further mischaracterized the teaching in Muza. As such, the Applicant submits that the rejection of claim 2 based on Muza is also improper. Hamano does not teach the features in claim 2 that are missing from Muza.

The Applicant submits therefore that this provides additional reasons for the allowability of claim 2 (and also claims 3-12, which depend variously from claim 2) over the cited references.

Claim 3

According to claim 3, a second differential transistor pair is connected between the first and second load devices and a second current sink such that the circuitry is adapted to provide a variable-gain amplifier (VGA) function.

In the non-limiting, exemplary embodiments of Figs. 2-3:

- Transistors M8 and M9 form an example of the second differential transistor pair of claim 3; and
- Current source I_{neg} is an example of the second current sink of claim 3.

In rejecting claim 3, the Examiner cited Fig. 1 in Muza. In particular, the Examiner stated, among other things, that transistors M11 and M14 in Muza's Fig. 1 form a second differential transistor pair connected between transistors M3 and M4 and current sink I2 such that the circuitry is adapted to provide a VGA function, where "M11 and M14 are adapted to adjusting the gain at the output nodes A1 and B1". For the following reasons, the Applicant submits that the Examiner mischaracterized the teachings in Muza in rejecting claim 3.

First of all, Muza's transistors M11 and M14 do not form a differential transistor pair connected between transistors M3 and M4 and current sink I2. Muza's transistors M11 and M12 may be said to form a differential transistor pair connected between transistors M3 and M4 and current sink I2 (and Muza's transistors M13 and M14 may be said to form another differential transistor pair), but not Muza's transistors M11 and M14.

Moreover, no combination of Muza's transistors M11-M14 provides a variable-gain amplifier function, as that term is used and understood by those of ordinary skill in the art. Rather, as described in column 4, line 41-64, Muza's transistors M11-M14 form part of a common-mode feedback circuit that regulates the voltages (not the gains) at nodes A1 and B1 to maintain their common-mode voltage based on the reference voltage V_{D1} at node D1. This is simply not a VGA function.

For at least this reason, the Applicant submits that the Examiner further mischaracterized the teaching in Muza. As such, the Applicant submits that the rejection of claim 3 based on Muza is also improper. Hamano does not teach the features in claim 3 that are missing from Muza.

The Applicant submits therefore that this provides additional reasons for the allowability of claim 3 (and also claims 4-8, which depend variously from claim 3) over the cited references.

In view of the above remarks, the Applicant believes that the pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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